[SPECIFICATION]

[TITLE OF THE INVENTION]

PLASMA DISPLAY PANEL AND DRIVING MEHTOD THEREOF

[BRIEF DESCRIPTION OF THE DRAWINGS]

Fig. 1 is a schematic diagram of a driver circuit according to prior art.

Fig. 2 is a timing diagram showing a driving operation of the driver circuit according to prior art.

Fig. 3 is a schematic diagram of a plasma display panel according to the present invention.

Figs. 4, 7, and 10 are circuit diagrams showing a driver circuit of a plasma display panel according to first to third embodiments of the present invention, respectively.

Figs. 5A and 5B are illustrations showing a current path in each mode of the driver circuit according to the first embodiment of the present invention.

Figs. 6 and 9 are timing diagrams showing a driving operation of the driver circuits according to the first and second embodiments of the present invention, respectively.

Figs. 8A to 8H are illustrations showing a current path in each mode of the driver circuit according to the second embodiment of the present invention.

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND PRIOR ARTS OF THE FIELD]

The present invention relates to an apparatus and method for driving a plasma display panel (PDP).

In recent years, flat panel displays such as liquid crystal displays (LCD), field

emission displays (FED), PDPs, and the like have been actively developed. The PDP is advantageous over other flat panel displays in regard to its high luminance, high luminous efficiency, and wide view angle, and accordingly, it is favorable for making a large-scale screen of more than 40 inches as a substitute for the conventional cathode ray tube (CRT).

The PDP is a flat panel display that uses plasma generated by gas discharge to display characters or images, and it includes, according to its size, more than several scores to millions of pixels arranged in a matrix pattern. Such a PDP is classified as a direct current (DC) type and an alternating current (AC) type according to its discharge cell structure and the waveform of the driving voltage applied thereto.

The DC PDP has electrodes exposed to a discharge space, allowing a DC to flow through the discharge space while voltage is applied, and hence it requires resistors for limiting the current. Contrarily, the AC PDP has electrodes covered with a dielectric layer that naturally forms a capacitance component that limits the current and protects the electrodes from the impact of ions during a discharge. Thus the AC PDP is superior to the DC PDP in regard to long lifetime.

Typically, the driving method of an AC PDP is sequentially composed of a reset step, an addressing step, a sustain discharge step, and an erase step.

In the reset step, the state of each cell is initialized in order to readily perform an addressing operation on the cell. In the addressing step, wall charges are accumulated on selected “on”-state cells and other “on”-state cells (i.e., addressed cells) for selecting “off”-state cells on the panel. In the sustain discharge step, a sustain pulse is applied alternately to scan electrodes (hereinafter referred to as “Y electrodes”) and sustain electrodes (hereinafter referred to as “X electrodes”) to perform a discharge for displaying an image on addressed cells.

In the AC PDP, the Y and X electrodes for such a sustain discharge act as a

capacitive load, and a capacitance exists for the Y and X electrodes (hereinafter referred to as "panel capacitor C_p").

Now, a description will be given as to a driver circuit for a conventional AC type PDP and its driving method.

Figs. 1 and 2 are illustrations showing a conventional driver circuit and its operating waveform.

The driver circuit generating a sustain pulse as suggested by Kishi et al. (Japanese Patent No. 3,201,603) comprises, as shown in Fig. 1, Y electrode driver 11, X electrode driver 12, Y electrode power supplier 13, and X electrode power supplier 14. X electrode driver 12 and X electrode power supplier 14 are the same in construction as Y electrode driver 11 and Y electrode power supplier 13, and will not be described in detail in the following description.

Y electrode power supplier 13 comprises capacitor C_1, and three switches SW_1, SW_2, and SW_3. Y electrode driver 11 comprises two switches SW_4 and SW_5. Switches SW_1 and SW_2 in the Y electrode power supplier 13 are coupled in series between power source $V_s/2$ and ground terminal GND. One terminal of capacitor C_1 is coupled to the contact of switches SW_1 and SW_2, and switch SW_3 is coupled between the other terminal of capacitor C_1 and ground terminal.

Switches SW_4 and SW_5 of Y electrode driver 11 are coupled in series to both terminals of capacitor C_1 of Y electrode power supplier 13. The contact of switches SW_4 and SW_5 is coupled to panel capacitor C_p.

As shown in Fig. 2, when switches SW_4, and SW_4' are turned on after switches SW_1, SW_3, and SW_2' are turned on and switches SW_2, SW_4, and SW_5 are turned off, Y electrode voltage V_y is increased to $V_s/2$ and capacitor C_1 is charged with the voltage $V_s/2$.

Subsequently, when switch SW_4 is turned off and switch SW_5 is turned on, the

Y electrode voltage V_y is decreased to ground voltage. Next, when switches SW_1, SW_3, and SW_4 are turned off and switches SW_2 and SW_5 are turned on, the Y electrode voltage V_y is decreased to $-V_s/2$ by the voltage $V_s/2$ charged in capacitor C_1. In addition, in next timing, when switch SW_5 is turned off and switch SW_4 is turned on, the Y electrode voltage V_y is increased to ground voltage.

Through this driving operation, positive voltage $+V_s/2$ and negative voltage $-V_s/2$ can be alternately applied to the Y electrodes. Likewise, positive voltage $+V_s/2$ and negative voltage $-V_s/2$ can be alternately applied to the X electrodes. The voltages $\pm V_s/2$ respectively applied to the X and Y electrodes have an inverted phase with respect to each other. By generating a sustain pulse swinging between $-V_s/2$ and $+V_s/2$, the potential difference between X and Y electrodes can be maintained at the sustain discharge voltage V_s.

Such a driver circuit can employ elements of a low withstand voltage, because the withstand voltage of each element in the circuit is $V_s/2$. However this driver circuit is applicable only to plasma display panels using a pulse swinging between $-V_s/2$ and $+V_s/2$.

In addition, the capacitor for storing the voltage used as a negative voltage in this circuit must has a large capacity, so that a considerable amount of an inrush current flows in an initial starting step due to the capacitor.

[PROBLEMS TO BE SOLVED OF THE INVENTION]

In accordance with the present invention, a PDP driving circuit for using switches having the low withstand voltage is provided.

[STRUCTURES OF THE INVENTION]

In one aspect of the present invention, a PDP is provided. In the PDP, first and second switches are coupled in series between a first power source for supplying a first voltage and a first terminal of the panel capacitor, and third and fourth switches

are coupled in series between the first terminal of the panel capacitor and a second power source for supplying a second voltage. A first capacitor is coupled between a contact of the first and second switches and a contact of the third and fourth switches. A fifth switch is coupled between the first capacitor and a third power source supplying a third voltage.

Preferably, the fifth switch is turned on so that the first capacitor is charged to the difference between the first and third voltages, and the third voltage is substantially a middle voltage between the first and second voltages.

The PDP further includes at least one inductor coupled to the first terminal of the panel capacitor; and sixth and seventh switches coupled in parallel between the inductor and the third power source. It is preferable that the first to fourth switches have a body diode.

The PDP may further include: sixth and seventh switches coupled in series between the first power source and a second terminal of the panel capacitor; eighth and ninth switches coupled in series between the second terminal of the panel capacitor and the second power source; a second capacitor coupled between a contact of the sixth and seventh switches and a contact of the eighth and ninth switches; and a tenth switch coupled between the second capacitor and the third power source.

In another aspect of the present invention, a PDP is provided. In the PDP, first and second switches are coupled in series between a first power source supplying a first voltage and a first terminal of the panel capacitor, and third and fourth switches are coupled in series between the first terminal of the panel capacitor and a second power source supplying a second voltage. A first signal line is coupled to a contact of the first and second switches, and a second signal line is coupled to a contact of the third and fourth switches. A voltage between the first and second signal lines is a third

voltage. The first and second voltages are alternately applied to the first terminal of the panel capacitor.

It is preferable that the third voltage is substantially a middle voltage between the first and second voltages.

Preferably, the PDP further includes a capacitor coupled between the first and second signal lines and charged to the third voltage. A fifth switch may be coupled between a third power source supplying a voltage substantially corresponding to a summation of the second and third voltages, and be turned on thereby charging the capacitor to the third voltage in the on state of the fourth switch.

The PDP preferably includes a power recovery section which comprises at least one inductor coupled to the first terminal of the panel capacitor. The power recovery section changes a terminal voltage of the panel capacitor using a resonance generated between the inductor and the panel capacitor.

In still another aspect of the present invention, a method for driving a PDP is provided, the PDP being driven by alternately applying first and second voltages through first and second signal lines coupled to a first terminal of a panel capacitor. The method includes: applying a third voltage between a contact of first and second switches formed on the first signal lines and a contact of third and fourth switches formed on the second signal lines, while the first voltage is applied to the first terminal of the panel capacitor by turning on the first and second switches; and applying the third voltage between the contact of the first and second switches and the contact of the third and fourth switches, while the second voltage is applied to the first terminal of the panel capacitor by turning on the third and fourth switches.

Preferably, a capacitor coupled between the contact of the first and second switches and the contact of the third and fourth switches is charged to the third voltage.

In the following detailed description, only the preferred embodiment of the

invention has been shown and described, simply by way of illustration of the best mode contemplated by the inventor(s) of carrying out the invention. As will be realized, the invention is capable of modification in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

In the specification, similar parts are denoted by the same reference numerals. When a part is coupled to another part, the part is not only directly connected to another part but is also electrically connected to another part while another device intervenes between them.

First, reference will be made to Fig. 3 to describe the schematic structure of a PDP according to an embodiment of the present invention.

Fig. 3 is a schematic of the PDP according to the embodiment of the present invention.

The PDP according to the embodiment of the present invention comprises, as shown in Fig. 3, plasma panel 100, address driver 200, scan/sustain driver 300, and controller 400.

Plasma panel 100 comprises a plurality of address electrodes A_1 to A_m arranged in columns, and a plurality of scan electrodes (hereinafter referred to as "Y electrodes") Y_1 to Y_n and sustain electrodes (hereinafter referred to as "X electrodes") X_1 to X_n alternately arranged in rows. Address driver 200 receives an address drive control signal from controller 400, and applies a display data signal for selection of discharge cells to be displayed to the individual address electrodes. Scan/sustain driver 300 receives a sustain discharge control signal from controller 400, and applies a sustain discharge pulse alternately to the X and Y electrodes. The input sustain discharge pulse applied causes a sustain discharge on the selected discharge cells. Controller 400 receives an external picture signal, generates the address drive control

signal and the sustain discharge control signal, and applies them to address driver 200 and scan/sustain driver 300, respectively.

Below is a description of a driver circuit of scan/sustain driver 300 according to a first embodiment of the present invention with reference to Figs. 4 to 6.

Fig. 4 is a circuit diagram of the driver circuit according to the first embodiment of the present invention. Figs. 5A and 5B are illustrations showing a current path in each mode of the driver circuit according to the first embodiment of the present invention, and Fig. 6 is a timing diagram showing a driving operation of the driver circuits according to the first embodiment of the present invention.

The driver circuit according to the first embodiment of the present invention comprises, as shown in Fig. 4, Y electrode driver 310, X electrode driver 320, Y electrode clamping section 330, and X electrode clamping section 340.

Y electrode driver 310 and X electrode driver 320 are coupled to each other with panel capacitor C_p therebetween. Y electrode driver 310 comprises switches Y_s and Y_h coupled in series between power source $V_s/2$ and the Y electrodes of panel capacitor C_p, and switches Y_L and Y_g are coupled in series between the Y electrodes of panel capacitor C_p and the power source $-V_s/2$.

Likewise, X electrode driver 320 comprises switches X_s and X_h coupled in series between power source $V_s/2$ and the X electrodes of panel capacitor C_p, and switches X_L and X_g coupled in series between the X electrodes of panel capacitor C_p and power source $-V_s/2$.

Y clamping section 330 comprises switch Y_u and capacitor C_1. Switch Y_u is coupled between a contact of switches Y_s and Y_h and ground terminal 0, and capacitor C_1 is coupled between the contact of switches Y_s and Y_h and a contact of switches Y_L and Y_g. Likewise, X clamping section 340 comprises switch X_u and capacitor C_2. Switch X_u is coupled between a contact of switches X_s and X_h and ground terminal 0,

and capacitor C_2 is coupled between the contact of switches X_s and X_h and a contact of switches X_L and X_g.

Although switches Y_s, Y_h, Y_L, Y_g, Y_u, X_s, X_h, X_L, X_g, and X_u included in Y and X electrode drivers 310 and 320 and Y and X clamping sections 330 and 340 are denoted as MOSFETs in Fig. 4, they are not specifically limited to MOSFETs, and may include any switches that perform the same or similar functions. Preferably, the switches have a body diode.

Below is a description of a driving method of the driver circuit according to the first embodiment of the present invention with reference to Figs. 5A, 5B, and 6.

In the first embodiment of the present invention, it is assumed that the voltages supplied by power sources $V_s/2$ and $-V_s/2$ are $V_s/2$ and $-V_s/2$, respectively, and that capacitors C_1 and C_2 are charged to voltage $V_s/2$. It is also assumed that voltage $V_s/2$ is a half of sustain discharge voltage V_s necessary for a sustain discharge of the panel.

First, as shown in Fig 6, in mode 1 (M1), switches Y_s, Y_h, X_g, X_L, and X_u are turned on, with switches X_s, X_h, Y_g, Y_L, and Y_u off.

As shown in Fig 5A, switches Y_s and Y_h in the on state cause voltage $V_s/2$ of power source $V_s/2$ to be applied to the Y electrodes of panel capacitor C_p, and switches X_L and X_g in the on state cause voltage $-V_s/2$ of power source - $V_s/2$ to be applied to the X electrodes of panel capacitor C_p. Y and X electrode voltages V_y and V_x of panel capacitor C_p are $V_s/2$ and $-V_s/2$, respectively, so that the voltage applied to both terminals of panel capacitor C_p is sustain discharge voltage V_s. When switch X_u is turned on, capacitor C_2 is charged and clamped to voltage $V_s/2$ by power source $-V_s/2$ and ground terminal 0.

The voltage of both terminals of switch Y_L is clamped to voltage $V_s/2$ stored in capacitor C_1 by the switch Y_h in the on state. Switches Y_s and Y_h in the on state cause

the voltage difference V_s between power sources $V_s/2$ and $-V_s/2$ to be applied to switches Y_L and Y_g. The voltage of both terminals of switch Y_g is clamped to voltage $V_s/2$ since the voltage of both terminals of switch Y_L is clamped to voltage $V_s/2$.

Likewise, the voltage of both terminals of switch X_h is clamped to voltage $V_s/2$ stored in capacitor C_2 by switch X_L in the on state. Switches X_L and X_g in the on state cause the voltage difference V_s between power sources $V_s/2$ and $-V_s/2$ to be applied to switches X_s and X_h. The voltage of both terminals of switch X_s is clamped to voltage $V_s/2$ since the voltage of both terminals of switch X_h is clamped to voltage $V_s/2$.

Accordingly, the withstand voltages of switches Y_L, Y_g, X_s, and X_h in the off state are clamped to $V_s/2$ in mode 1.

Next, as shown in Fig 6, in mode 2 (M2), switches X_s, X_h, Y_g, Y_L, and Y_u are turned on, with switches Y_s, Y_h, X_g, X_L, and X_u off.

As shown in Fig 5B, switches Y_g and Y_L in the on state cause voltage $-V_s/2$ of power source $-V_s/2$ to be applied to the Y electrodes of panel capacitor C_p, and switches X_s and X_h in the on state cause voltage $V_s/2$ of power source $V_s/2$ to be applied to the X electrodes of panel capacitor C_p. Therefore, Y and X electrode voltages V_y and V_x of panel capacitor C_p are $-V_s/2$ and $V_s/2$, respectively, so that the voltage applied to both terminals of panel capacitor C_p is V_s.

As described in mode 1 (M1), the voltage of both terminals of switch Y_h is clamped to voltage $V_s/2$ stored in capacitor C_1 by switch Y_L in the on state. Since switch Y_h is clamped to voltage $V_s/2$ and switches Y_L and Y_g are in the on state, the voltage of both terminals of switch Y_s is clamped to $V_s/2$ by power sources $V_s/2$ and $-V_s/2$. Likewise, switch X_L is clamped to voltage $V_s/2$ stored in capacitor C_2, and switch X_g is clamped to voltage $V_s/2$ by power sources $V_s/2$ and $-V_s/2$.

According to the first embodiment of the present invention, the voltage applied to switches Y_s, Y_h, X_L, and X_g and switches Y_L, Y_g, X_s, and X_h is clamped to $V_s/2$ by

capacitors C_1 and C_2, respectively, while the voltage of both terminals of panel capacitor C_p is maintained to voltage V_s. Furthermore, a high inrush current hardly occurs in the initial starting step, because capacitors C_1 and C_2 are not used for applying a negative voltage to the Y or X electrodes of panel capacitor C_p.

Because of the capacitance component of panel capacitor C_p, a reactive power as well as the power for a discharge is required in applying a waveform for a sustain discharge. A circuit for recovering the reactive power and reusing it is called "power recovery circuit". Below is a description of another embodiment having a power recovery circuit added to the driver circuit according to the first embodiment of the present invention with reference to Figs. 7 to 9.

Fig. 7 is a circuit diagram of a driver circuit according to a second embodiment of the present invention.

The driver circuit according to the second embodiment of the present invention further comprises, as shown in Fig. 7, Y and X electrode power recovery sections 350 and 360 added to the driver circuit according to the first embodiment of the present invention.

Y electrode power recovery section 350 comprises inductor L_1 and switches Y_r and Y_f. Inductor L_1 is coupled to a contact of switches Y_h and Y_L, i.e., the Y electrodes of panel capacitor C_p, and switches Y_r and Y_f are coupled in parallel between inductor L_1 and ground terminal 0. Y electrode power recovery section 350 further comprises diodes D_1 and D_2 coupled between switch Y_r and inductor L_1 and between switch Y_f and inductor L_1, respectively. Diodes D_1 and D_2 interrupt current paths that may be formed by body diodes of switches Y_r and Y_f, respectively.

X electrode power recovery section 360 comprises inductor L_2 and switches X_r and X_f, and additionally includes diodes D_3 and D_4. X electrode power recovery section 360 is the same in construction as Y electrode power recovery section 350 and will not

be described in detail. Switches Y_r, Y_f, X_r, and X_f of Y and X electrode power recovery sections 350 and 360 may comprise MOSFETs.

Below is a description of a driving method of the driver circuit according to the second embodiment of the present invention with reference to Figs. 8A to 8H and 9.

Figs. 8A to 8H are illustrations showing a current path in each mode of the driver circuit according to the second embodiment of the present invention, and Fig. 9 is a timing diagram showing a driving operation of the driver circuits according to the second embodiment of the present invention.

In the second embodiment of the present invention, it is assumed that before the start of the mode 1 (M1), switches Y_s, Y_h, X_g, X_L, and X_u are in the on state, with switches X_s, X_h, Y_g, Y_L, Y_u, X_r, Y_f, X_f, and Y_r off. It is also assumed that capacitors C_1 and C_2 are charged to voltage $V_s/2$ and that the inductance of inductors L_1 and L_2 is L.

As shown in Figs. 8A and 9, Before the start of mode 1, current path 81 is formed that includes power source $V_s/2$, switches Y_s and Y_h, panel capacitor C_p, switches X_L and X_g, and power source $-V_s/2$. Then Y electrode voltage V_y of panel capacitor C_p is sustained at $V_s/2$ due to power source $V_s/2$, and X electrode voltage V_x of panel capacitor C_p is sustained at $-V_s/2$ due to power source $-V_s/2$. Capacitor C_2 is clamped to $V_s/2$ due to current path 82 which includes ground terminal 0, switch X_u, the capacitor C_2, switch X_g, and power source $-V_s/2$. The withstand voltages of the switches Y_L and Y_g are clamped to $V_s/2$ due to the voltage $V_s/2$ stored in capacitor C_1, and the withstand voltages of the switches X_s and X_h are clamped to $V_s/2$ due to the voltage $V_s/2$ stored in capacitor C_2, as described in the first embodiment.

When switches Y_f and X_f are turned on, formed are current path 83 which includes power source $V_s/2$, switch Y_s and Y_h, inductor L_1, diode D_2, switch Y_f, and ground terminal 0, and current path 84 that includes ground terminal 0, switch X_r, diode D_3, inductor L_2, switches X_L and X_g, and power source $-V_s/2$. The magnitude of

currents I_{L1} and I_{L2} flowing to the inductors L_1 and L_2 is linearly increased with a slope of $V_s/2L$ through current paths 82 and 83. Due to currents I_{L1} and I_{L2}, energy is stored in inductors L_1 and L_2.

In mode 2 (M2), with switches Y_f and X_r on, switches Y_s, Y_h, X_g, X_L, and X_u are turned off. Then, as shown in Fig. 8B, current path 85 is formed that includes switch X_r, diode D_3, inductor L_2, panel capacitor C_p, inductor L_1, diode D_2, and switch Y_f, so that an LC resonance current flows due to inductors L_1 and L_2 and panel capacitor C_p. With this LC resonance current, Y electrode voltage V_y of panel capacitor C_p is reduced to $-V_s/2$ and X electrode voltage V_x is increased to $V_s/2$. Y electrode voltage V_y does not exceed $-V_s/2$ due to the body diodes of switches Y_L and Y_g, and X electrode voltage V_x does not exceed $V_s/2$ due to the body diodes of switches X_s and X_h.

As described above, energy is previously stored in inductors L_1 and L_2, and the stored energy and the LC resonance current are used for changing Y and X electrode voltages V_y and V_x of panel capacitor C_p. Thus Y and X electrode voltages V_y and V_x can be changed to $V_s/2$ and $-V_s/2$, respectively, even in the actual circuit including parasitic components.

In mode 3 (M3), when Y and X electrode voltages V_y and V_x of the panel capacitor C_p are $-V_s/2$ and $V_s/2$, respectively, the switches X_s, X_h, Y_g, and Y_L are turned on. Then, as shown in Fig. 8C, path 86 is formed that includes power source $V_s/2$, switches X_s and X_h, panel capacitor C_p, switches Y_L and Y_g, and power source $-V_s/2$, and Y and X electrode voltages V_y and V_x of panel capacitor C_p are sustained at $V_s/2$ and $-V_s/2$, respectively.

Current I_{L1} flowing to inductor L_1 is recovered to ground terminal 0 through path 87 which includes the body diodes of switches Y_g and Y_L, inductor L_1, diode D_2, and switch Y_f. Current I_{L2} flowing to inductor L_2 is recovered to power source $V_s/2$ through path 88 which includes switch X_r, diode D_3, inductor L_2, and the body diodes of

switches X_h and X_s. Therefore, the magnitude of currents I_{L1} and I_{L2} is linearly reduced to 0A with a slope of $V_s/2L$.

When switch Y_u is turned on, capacitor C_1 is charged and clamped to voltage $V_s/2$ through loop 89 which includes ground terminal 0, switch Y_u, capacitor C_1, switch Y_g, and power source $-V_s/2$. As described in the first embodiment, the withstand voltages of switches Y_s and Y_h are clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_1, respectively, and the withstand voltages of switches X_L and X_g are clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_2, respectively.

In mode 4 (M4), when currents I_{L1} and I_{L2} are 0A, switches Y_f and Xr are turned off so that paths 87 and 88 are interrupted. As shown in Fig. 8D, Y and X electrode voltages V_y and V_x are still sustained at $-V_s/2$ and $V_s/2$, respectively, due to switches Y_L, Y_g, X_s, and X_h which are turned on . In addition, the withstand voltagés of switches Y_s, Y_h, X_L, and X_g are clamped to $V_s/2$ as described in mode 3 (M3).

In mode 5 (M5), energy is stored in inductors L_1 and L_2 while Y and X electrode voltages V_y and V_x of panel capacitor C_p are sustained at $-V_s/2$ and $V_s/2$. In detail, when switches Y_r and X_f are turned on, current path 90 is formed that includes ground terminal 0, switch Y_r, diode D_1, inductor L_1, switches Y_L and Y_g, and power source $-V_s/2$, and current path 91 is formed that includes power source $V_s/2$, switches X_s and X_h, inductor L_2, diode D_4, switch X_f, and ground terminal 0, as shown in Fig. 8E. By current paths 90 and 91, currents I_{L1} and I_{L2} flowing to inductors L_1 and L_2 are linearly increased with a slope of $V_s/2L$. The energy is stored in inductors L_1 and L_2 due to currents I_{L1} and I_{L2}.

In mode 6 (M6), with the switches Y_f and X_r on, switches X_s, X_h, Y_g, Y_L, and X_u are turned off after the energy is stored in inductors L_1 and L_2. Then path 92 is formed that includes switch Y_r, diode D_1, inductor L_1, panel capacitor C_p, inductor L_2, diode D_4, and switch X_f. Path 92 makes an LC resonance current flow due to the inductors L_1

and L_2 and the panel capacitor C_p. With this LC resonance current, Y electrode voltage V_y of panel capacitor C_p is increased to $V_s/2$ and X electrode voltage V_x is decreased to $-V_s/2$. Y electrode voltage V_y does not exceed $V_s/2$ due to the body diode of switches Y_s and Y_h, and X electrode voltage V_x does not exceed $-V_s/2$ due to the body diode of switches X_L and X_g.

As described in mode 2 (M2), in mode (M6), after the energy is stored in inductors L_1 and L_2, Y and X electrode voltages V_y and V_x are changed by using this energy and the LC resonance current. Therefore Y and X electrode voltages V_y and V_x can be changed to $V_s/2$ and $-V_s/2$, respectively, even in the actual circuit including parasitic components.

In mode 7 (M7), when Y and X electrode voltages V_y and V_x are $V_s/2$ and $-V_s/2$, switches Y_s, Y_h, X_g, and X_L are turned on to sustain these voltages V_y and V_x. Then, path 81 is formed that includes power source $V_s/2$, switches Y_s and Y_h, panel capacitor C_p, switches X_L and X_g, and power source $-V_s/2$ so that Y and X electrode voltages V_y and V_x of panel capacitor C_p are sustained at $V_s/2$ and $-V_s/2$, respectively.

Current I_{L1} flowing to inductor L_1 is recovered to power source $V_s/2$ through path 93 that includes switch Y_r, diode D_1, inductor L_1, and the body diodes of switches Y_h and Y_s. Current I_{L2} flowing to inductor L_2 is recovered to ground terminal 0 through current path 94 that includes the body diodes of switches X_g and X_L, inductor L_2, diode D_4, and switch X_f.

In addition, when switch X_u is turned on, capacitor C_2 is charged and clamped to $V_s/2$ through path 82 which includes switch X_u, capacitor C_2, switch X_g, and power soured $-V_s/2$. As described above in regard to mode 1 (M1), the withstand voltages of switches Y_L and Y_g, are clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_1, and the withstand voltages of switches X_s and X_h are clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_2.

In mode 8 (M8), switches Y_r and X_f are turned off so that paths 93 and 94 are interrupted, when currents I_{L1} and I_{L2} flowing to inductors L_1 and L_2. Switches Y_s, Y_h, X_L, and X_g in the on state cause Y and X electrode voltages V_y and V_x of panel capacitor C_p to be still sustained at $V_s/2$ and $-V_s/2$, respectively. As described in mode 7 (M7), the withstand voltages of switches X_s, X_h, Y_L, and Y_g are clamped to $V_s/2$.

Subsequently, the cycle of modes 1 to 8 (M1-M8) is repeated to generate Y and X electrode voltages V_y and V_x swinging between $V_s/2$ and $-V_s/2$, thereby sustaining the potential difference between the X and Y electrodes at sustain discharge voltage of V_s.

Although each of Y and X electrode power recovery sections 350 and 360 has one inductor in the second embodiment of the present invention, all other differently modified power recovery sections may be used. For example, Y electrode power recovery section 350 may include inductors L_{11} and L_{12} each forming a different path. More specifically, energy is stored in the inductor L_{11} while Y electrode voltage V_y is sustained at $V_s/2$, and then used to change Y electrode voltage V_y to $-V_s/2$. Then, the energy stored in inductor L_{11} is recovered and energy is stored in inductor L_{12}, while Y electrode voltage V_y is sustained at $-V_s/2$. The energy stored in inductor L_{12} is used to change Y electrode voltage V_y to $V_s/2$.

Although the voltages supplied by power sources $V_s/2$ and $-V_s/2$ are $V_s/2$ and $-V_s/2$, respectively, in the first and second embodiments of the present invention, a different voltage can also be used as long as the voltage difference between two power sources $V_s/2$ and $-V_s/2$ is V_s which is necessary for sustain discharge. Namely, the voltages supplied by power sources $V_s/2$ and $-V_s/2$ can be V_h and (V_h-V_s) so that Y and X electrode voltages V_y and V_x swing between V_h and (V_h-V_s).

An exemplary third embodiment in which the voltages supplied by power sources of Fig. 4 are sustain discharge voltage V_s and ground voltage 0V, respectively,

will be described with reference to Fig. 10.

Fig. 10 is a circuit diagram showing a driver circuit of a plasma display panel according to the third embodiment of the present invention.

As shown in Fig. 10, in the driving circuit according the third embodiment, power sources $V_s/2_1$ and $V_s/2_2$ supply the voltages $V_s/2$, respectively. In detail, power sources $V_s/2_1$ and $V_s/2_2$ are coupled in series and supply voltage V_s. Switches Y_s and X_s are coupled to power sources $V_s/2_1$, and switches Y_g and X_g are coupled to ground terminal 0. Switches Y_u and X_u are a contact of power sources $V_s/2_1$ and $V_s/2_2$.

Except for the voltages applied to the Y and X electrode of panel capacitor C_p, the operation of the driver circuit according to the third embodiment of the present invention is the same to that of the first embodiment. In addition, capacitor C_1 is charged to $V_s/2$ when switch Y_u is turned on, and capacitor C_2 is charged to $V_s/2$ when switch X_u is turned on.

In detail, in mode 1, voltages V_s and 0V are applied to the Y and X electrode of panel capacitor C_p, respectively. The withstand voltage of switch Y_L is clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_1. The withstand voltage of switch Y_g is clamped to $V_s/2$ due to the voltage of both terminals $V_s/2$ of switch Y_g and voltage V_s supplied by serially coupled power sources $V_s/2_1$ and $V_s/2_2$. Likewise, the withstand voltage of switch X_h is clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_2. The withstand voltage of switch X_s is clamped to $V_s/2$ due to the voltage of both terminals $V_s/2$ of switch X_h and voltage V_s supplied by power sources $V_s/2_1$ and $V_s/2_3$.

In mode 2, voltages 0V and V_s are applied to the Y and X electrode of panel capacitor C_p, respectively. As described above, the withstand voltages of switches Y_s and Y_h are clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_1 and voltage V_s supplied by power sources $V_s/2_1$ and $V_s/2_2$. Likewise, the withstand voltages of switches X_L and X_g are clamped to $V_s/2$ due to voltage $V_s/2$ stored in capacitor C_2 and

voltage V_s supplied by power sources $V_s/2_1$ and $V_s/2_2$.

In addition, although the two switches are coupled between the power source and the X or Y electrode of panel capacitor C_p in the first to third embodiments of the present invention, the number of switches is not specifically limited in the present invention. For example, it is assumed that four switches S_1, S_2, S_3, and S_4 are coupled in series between power source $V_s/2$ and the Y electrode of panel capacitor C_p, and four switches S_5, S_6, S_7, and S_8 are coupled in series between power source $-V_s/2$ and the Y electrode of panel capacitor C_p. When the capacitor C_1 is coupled between the contact of switches S_2 and S_3 and the contact of switches S_6 and S_7, the withstand voltage of the switches S_1 and S_2, the switches S_3 and S_4, the switches S_5 and S_6, or the switches S_7 and S_8 is $V_s/2$.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

[EFFECT OF THE INVENTION]

According to the present invention, the withstand voltage of the switches can be half of voltage V_s necessary for sustain discharge, thereby reducing the production unit cost. The present invention also eliminates an inrush current generated when the voltage stored in an external capacitor is used in changing the terminal voltage of the panel capacitor. Furthermore, the driver circuit of the present invention can be used irrespective of the waveform of sustain pulses by changing the power source applied to it.